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APPLICATION FOR LETTERS PATENT

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**SEMICONDUCTOR PROCESSING METHODS OF
FORMING PHOTORESIST OVER SILICON NITRIDE
MATERIALS, AND SEMICONDUCTOR WAFER
ASSEMBLIES COMPRISING PHOTORESIST OVER
SILICON NITRIDE MATERIALS**

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1 SEMICONDUCTOR PROCESSING METHODS OF FORMING
2 PHOTORESIST OVER SILICON NITRIDE MATERIALS, AND
3 SEMICONDUCTOR WAFER ASSEMBLIES COMPRISING
4 PHOTORESIST OVER SILICON NITRIDE MATERIALS

5 RELATED PATENT DATA

6 This application is a continuation-in-part of U.S. Patent Application
7 Serial No. 09/057,155, filed April 7, 1998; and a continuation-in-part of
8 U.S. Patent Application Serial No. 09/252,642, filed April 20, 1999.

9 TECHNICAL FIELD

10 The invention pertains to methods of forming and patterning
11 photoresist over silicon nitride materials, and to semiconductor wafer
12 assemblies comprising photoresist over silicon nitride materials. The
13 invention also relates generally to semiconductor processing methods of
14 promoting adhesion of photoresist to an outer substrate layer
15 predominantly comprising silicon nitride.

16
17 BACKGROUND OF THE INVENTION

18 Silicon nitride is frequently utilized in modern semiconductor
19 fabrication methods. For instance, silicon nitride is an insulative
20 material, and can be utilized to electrically isolate conductive components
21 from one another. Also, silicon nitride is selectively etchable relative to
22 other materials utilized in semiconductor fabrication processes, such as,
23 for example, silicon dioxide, and is can thus be utilized as an etch stop

1 material. Another example use of silicon nitride is for LOCOS (LOCAl
2 Oxidation of Silicon). LOCOS comprises growing oxide over field
3 regions of a semiconductor substrate, while not growing the oxide over
4 other regions of the substrate. The other regions of the substrate are
5 typically protected by a thin layer of silicon nitride during the oxide
6 growth.

7 In many applications of silicon nitride, a silicon nitride layer is
8 patterned into a specific shape. An example prior art patterning process
9 is described with reference to Figs. 1-2. Referring to Fig. 1, a
10 semiconductor wafer fragment 10 comprises a substrate 12 covered by a
11 pad oxide layer 14, a silicon nitride layer 16, an antireflective coating 18,
12 and a photoresist layer 20.

13 Substrate 12 can comprise, for example, monocrystalline silicon
14 lightly doped with a p-type dopant. To aid in interpretation of the
15 claims that follow, the term "semiconductive substrate" is defined to mean
16 any construction comprising semiconductive material, including, but not
17 limited to, bulk semiconductive materials such as a semiconductive wafer
18 (either alone or in assemblies comprising other materials thereon), and
19 semiconductive material layers (either alone or in assemblies comprising
20 other materials). The term "substrate" refers to any supporting structure,
21 including, but not limited to, the semiconductive substrates described
22 above.
23

1 Pad oxide 14 is a thin layer (from about 40 to about
2 50 nanometers thick) of silicon dioxide, and is provided to alleviate
3 stresses that can be caused by silicon nitride layer 16. Pad oxide 14 can
4 be formed by exposing a silicon-comprising substrate 12 to an oxidizing
5 atmosphere.

6 Silicon nitride layer 16 can be formed over pad oxide 14 by, for
7 example, chemical vapor deposition. A thickness of silicon nitride
8 layer 16 will vary depending on the application of the silicon nitride
9 layer. In LOCOS fabrication processes, silicon nitride layer 16 will
10 typically be provided to a thickness of from about 100 nanometers to
11 about 200 nanometers.

12 Antireflective coating 18 is a polymer film provided over silicon
13 nitride layer 16 for two purposes. First, antireflective coating 18 absorbs
14 light during photolithographic patterning of photoresist layer 20. Such
15 absorption can prevent light that has passed through photoresist layer 20
16 from reflecting back into the layer to constructively or destructively
17 interfere with other light passing through layer 20. Second, antireflective
18 coating 18 functions as a barrier to prevent diffusion of nitrogen atoms
19 from silicon nitride layer 16 into photoresist layer 20. It is found that
20 if nitrogen atoms diffuse into photoresist 20, they can alter its sensitivity
21 to light (so-called "poisoning" of the photoresist).

22 Photoresist layer 20 is provided to form a pattern over silicon
23 nitride layer 16. Photoresist layer 20 comprises a polymer composition

1 which becomes selectively soluble in a solvent upon exposure to light.
2 If photoresist 20 comprises a negative photoresist, it is rendered insoluble
3 in a solvent upon exposure to light, and if it comprises a positive
4 photoresist, it is rendered soluble in solvent upon exposure to light.

5 Referring to Fig. 2, photoresist layer 20 is exposed to a patterned
6 beam of light to selectively render portions of the photoresist soluble in
7 a solvent, while leaving other portions insoluble. After such exposure,
8 the solvent is utilized to selectively remove portions of photoresist layer
9 20 and thereby convert photoresist layer 20 into the pattern shown.

10 Referring to Fig. 3, the pattern from layer 20 is transferred to
11 underlying layers 18, 16 and 14 by an appropriate etch. A suitable etch
12 can comprise, for example, a plasma-enhanced etch utilizing NF_3 and
13 HBr . In subsequent processing which is not shown, antireflective coating
14 layer 18 and photoresist layer 20 can be removed to leave stacks
15 comprising pad oxide 14 and silicon nitride 16 over substrate 12. The
16 stacks can then be utilized for subsequent fabrication processes. For
17 instance, the stacks can be utilized for LOCOS by subsequently exposing
18 wafer fragment 10 to oxidizing conditions to grow field oxide between
19 the stacks. As another example, conductive metal layers may be
20 provided between the stacks, and the stacks utilized for electrical
21 isolation of such metal layers.

22 The above-described processing sequence requires formation of four
23 distinct layers (14, 16, 18, and 20), each of which is formed by

1 processing conditions significantly different than those utilized for
2 formation of the other three layers. For instance, antireflective
3 coating 18 is commonly formed by a spin-on process, followed by a bake
4 to remove solvent from the layer. In contrast, silicon nitride layer 16
5 is typically formed by a chemical vapor deposition process. The spin-on
6 and baking of layer 18 will typically not occur in a common chamber as
7 the chemical vapor deposition of layer 16, as processing chambers are
8 generally not suited for such diverse tasks. Accordingly, after formation
9 of silicon nitride layer 16, semiconductor wafer fragment 10 is transferred
10 to a separate processing chamber for formation of antireflective coating
11 18. The semiconductive wafer fragment 10 may then be transferred to
12 yet another chamber for formation of photoresist layer 20.

13 A continuing goal in semiconductive wafer fabrication processes is
14 to minimize processing steps, and particularly to minimize transfers of
15 semiconductive wafers between separate processing chambers.
16 Accordingly, it would be desirable to develop alternative fabrication
17 processes wherein fabrication steps could be eliminated.

18 It has been attempted to pattern silicon nitride layers without
19 utilizing an antireflective coating over the layers. However, such creates
20 complications, such as those illustrated in Fig. 4. Identical numbering
21 is utilized in Fig. 4 as was utilized with reference to Figs. 1-3, with
22 differences indicated by the suffix "a". A difference between the
23 semiconductive wafer fragment 10a of Fig. 4 and the wafer fragment 10

1 of Figs. 1-3 is that antireflective coating 18 is eliminated from the wafer
2 fragment 10a construction. Wafer fragment 10a of Fig. 4 is shown at
3 a processing step analogous to the processing step shown in Fig. 2.
4 Elimination of antireflective coating layer 18 has enabled nitrogen atoms
5 to diffuse from silicon nitride layer 16 into a lower portion of
6 photoresist layer 20a. The nitrogen atoms have altered the photoresist
7 such that regions which should be removed by exposure to a solvent are
8 no longer removable by the solvent. This can render semiconductive
9 wafer fragment 10a unsuitable for the further processing described above
10 with reference to Fig. 3. It would be desirable to develop alternative
11 methods of forming photoresist over silicon nitride which avoid the
12 adverse effects illustrated in Fig. 4.

13 Traditional silicon nitride layers have stoichiometries of about Si_3N_4 .
14 Silicon enriched silicon nitride layers (i.e., silicon nitride layers having
15 a greater concentration of silicon than Si_3N_4 , such as, for example, Si_4N_4)
16 have occasionally been used in semiconductor fabrication processes. The
17 silicon enriched silicon nitride was utilized as a layer having a
18 substantially homogenous composition throughout its thickness, although
19 occasionally a small portion of the layer (1% or less of a thickness of
20 the layer) was less enriched with silicon than the remainder of the layer
21 due to inherent deposition problems.

22 When the silicon enriched silicon nitride layers were utilized in a
23 process such as that shown in Fig. 4 (i.e., a process wherein no

1 antireflective coating layer is provided between the silicon nitride and the
2 photoresist), it was found that good photolithographic patterning of the
3 photoresist could be obtained. However, it was also found that the
4 silicon nitride was difficult to pattern due to a resistance of the silicon
5 nitride to etching. Accordingly, it would be desired to develop
6 alternative methods of utilizing silicon nitride in wafer fabrication
7 processes.

8 In additional aspect of the prior art, microcircuit fabrication
9 involves provision of precisely controlled quantities of impurities into
10 small regions of a silicon substrate, and subsequently interconnecting
11 these regions to create components and integrated circuits. The patterns
12 that define such regions are typically created by a photolithographic
13 process. Such processing sets the horizontal dimensions on the various
14 parts of the devices and circuits. Photolithography is a multistep pattern
15 transfer process similar to stenciling or photography. In photolithography,
16 the required pattern is first formed in reticles or photomasks and
17 transferred into the surface layer(s) of the wafer through photomasking
18 steps.

19 Inherent in photolithography is application and adherence of
20 photoresist materials to underlying substrates. The resist must be
21 capable of adhering to these surfaces through all the resist processing
22 and etch steps. Poor adhesion brings about severe undercutting, loss of
23 resolution, or possibly the complete loss of the pattern. Wet etching

1 techniques demand a high level of adhesion of the resist film to the
2 underlying substrates.

3 Various techniques are used to increase the adhesion between resist
4 and a substrate such as, a) dehydration baking prior to coating; b) use
5 of hexamethyldisilazane (HMDS) and vapor priming systems to promote
6 resist adhesion for polysilicon, metals and SiO₂ layers, and c) elevated
7 temperature post-bake cycles. HMDS functions as an effective adhesion
8 promoter for silicon and silicon oxide containing films, but provides
9 effectively no surface-linking adhesion promotion with respect to silicon
10 nitride films.

11 Accordingly, it would be desirable to develop alternate and
12 improved techniques for providing better adhesion of photoresist to
13 silicon nitride films.

14 15 SUMMARY OF THE INVENTION

16 In one aspect, the invention encompasses a semiconductor
17 processing method of forming a photoresist over a silicon nitride
18 material. The silicon nitride material has a surface. A barrier layer
19 comprising silicon and nitrogen is formed over the surface. The
20 photoresist is formed over and against the barrier layer.

21 In another aspect, the invention encompasses a semiconductor
22 processing method of forming and patterning a photoresist layer over a
23 silicon nitride material. The silicon nitride material has a surface. A

1 barrier layer comprising silicon and nitrogen is formed over the surface.
2 The photoresist is formed over and against the barrier layer. The
3 photoresist is exposed to a patterned beam of light to render at least
4 one portion of the photoresist more soluble in a solvent than an other
5 portion. The barrier layer is an antireflective surface that absorbs light
6 passing through the photoresist. The photoresist is exposed to the
7 solvent to remove the at least one portion while leaving the other
8 portion over the barrier layer.

9 In yet another aspect, the invention encompasses a semiconductor
10 wafer assembly. The assembly includes a silicon nitride material, a
11 barrier layer over a surface of the material, and a photoresist over and
12 against the barrier layer. The barrier layer comprises silicon and
13 nitrogen.
14

15 BRIEF DESCRIPTION OF THE DRAWINGS

16 Preferred embodiments of the invention are described below with
17 reference to the following accompanying drawings.

18 Fig. 1 is a diagrammatic, fragmentary, cross-sectional view of a
19 semiconductor wafer fragment at a preliminary step of a prior art
20 processing sequence.

21 Fig. 2 is a view of the Fig. 1 wafer fragment shown at a
22 processing step subsequent to that of Fig. 1.
23

1 Fig. 3 is a view of the Fig. 1 wafer fragment shown at a
2 processing step subsequent to that of Fig. 2.

3 Fig. 4 is a diagrammatic, fragmentary, cross-sectional view of a
4 prior art wafer fragment processed according to a second prior art
5 processing sequence.

6 Fig. 5 is a diagrammatic, fragmentary, cross-sectional view of a
7 semiconductor wafer fragment at a preliminary processing step of a
8 method of the present invention.

9 Fig. 6 is a view of the Fig. 5 wafer fragment shown at a
10 processing step subsequent to that of Fig. 5.

11 Fig. 7 is a view of the Fig. 5 wafer fragment shown at a
12 processing step subsequent to that of Fig. 6.

13 Fig. 8 is a view of the Fig. 5 wafer fragment shown at a
14 processing step subsequent to that of Fig. 7.

15 Fig. 9 is a diagrammatic sectional view of a semiconductor wafer
16 fragment at one processing step in accordance with the invention.

17 Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step
18 subsequent to that shown by Fig. 9.

19 Fig. 11 is a view of the Fig. 9 wafer fragment at a processing step
20 subsequent to that shown by Fig. 10.

21 Fig. 12 is a view of the Fig. 9 wafer fragment at a processing step
22 subsequent to that shown by Fig. 11.
23

1 Fig. 13 is a diagrammatic sectional view of an alternate
2 embodiment semiconductor wafer fragment at one alternate processing
3 step in accordance with the invention.

4 Fig. 14 is a view of the Fig. 13 wafer fragment at a processing
5 step subsequent to that shown by Fig. 13.

6 Fig. 15 is a diagrammatic sectional view of yet another alternate
7 embodiment semiconductor wafer fragment at yet another alternate
8 processing step in accordance with the invention.

9 10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

11 This disclosure of the invention is submitted in furtherance of the
12 constitutional purposes of the U.S. Patent Laws "to promote the progress
13 of science and useful arts" (Article 1, Section 8).

14 A semiconductor processing method of the present invention is
15 described with reference to Figs. 5-8. Referring first to Fig. 5, a
16 semiconductor wafer fragment 30 comprises a substrate 32, a pad oxide
17 layer 34 and a silicon nitride layer 36. Substrate 32 and pad oxide
18 layer 34 can comprise identical compositions to those discussed above in
19 the "background" section regarding prior art substrate 12 and prior art
20 pad oxide 14. Silicon nitride layer 36 differs from the prior art silicon
21 nitride layer 16 (discussed in the "background" section) in that silicon
22 nitride layer 36 comprises two distinct portions 38 and 40, having
23 different compositions. A dashed line 39 is utilized to indicate an

1 interface between portions 38 and 40. Portion 40 is a nitrogen barrier
2 layer formed over portion 38, and is preferably thinner than portion 38
3 so that the majority of silicon nitride layer 36 has the properties of
4 portion 38. Portion 40 can comprise, for example, a thickness of less
5 than or equal to about 5 nanometers, and portion 38 can comprise, for
6 example, a thickness of greater than 95 nanometers.

7 Each of portions 38 and 40 preferably comprises silicon and
8 nitrogen, but portion 40 preferably comprises a lower percentage of
9 nitrogen than portion 38. Portion 38 can comprise, for example, a
10 traditional silicon nitride composition, such as a composition having a
11 stoichiometry of about Si_3N_4 . Such traditional silicon nitride material can
12 be formed by, for example, chemical vapor deposition. Portion 40 can
13 comprise, for example, a silicon nitride material enriched in silicon
14 relative to the material of portion 38. For example, portion 40 can
15 comprise a stoichiometry of Si_xN_y , where in x is greater than or equal
16 to y. Example stoichiometries of portion 40 are Si_4N_4 , Si_7N_4 and Si_{10}N_1 .

17 Portion 40 is preferably formed from a silicon precursor gas and
18 a nitrogen precursor gas in a common and uninterrupted deposition
19 process with portion 38. By "common deposition process" it is meant a
20 deposition process wherein a wafer is not removed from a reaction
21 chamber between the time that an initial portion of a silicon nitride
22 layer is formed and the time that a final portion of the silicon nitride
23 layer is formed. By "uninterrupted deposition process" it is meant a

1 process wherein the flow of at least one of the silicon precursor gas and
2 the nitrogen precursor gas does not stop during the deposition process.

3 An example deposition process for forming silicon nitride layer 36
4 is a chemical vapor deposition (CVD) process utilizing SiH_2Cl_2
5 (dichlorosilane) as a silicon precursor gas, and NH_3 (ammonia) as a
6 nitrogen precursor gas. Substrate 32 is provided within a CVD reaction
7 chamber, together with the dichlorosilane and ammonia. A pressure
8 within the chamber is, for example, from about 100 mTorr to
9 about 1 Torr, and a temperature within the chamber is, for example,
10 from about 700° C to about 800° C.

11 The dichlorosilane and ammonia are provided in the chamber to
12 a first ratio, and such first ratio is utilized to deposit portion 38. The
13 first ratio can be, for example, 0.33 to form a portion 38 have a
14 stoichiometry of about Si_3N_4 . After portion 38 is formed, the ratio of
15 dichlorosilane to ammonia is altered to a second ratio having an
16 increased relative amount of dichlorosilane. Such second ratio of
17 dichlorosilane to ammonia is utilized to form second portion 40. An
18 example second ratio is about 6, which forms a silicon nitride portion 40
19 having a stoichiometry of Si_xN_y , wherein the ratio of x to y is greater
20 than 1.

21 An alternative method of forming a nitrogen barrier portion 40 of
22 silicon nitride layer 36 is to form the portion 40 from silicon, oxygen
23 and nitrogen. For instance, portion 40 can comprise silicon oxynitride

1 having a stoichiometry of $\text{Si}_x\text{N}_y\text{O}_z$, wherein x, y and z are greater than
2 or equal to 1 and less than or equal to 5. An example composition of
3 the silicon oxynitride is $\text{Si}_3\text{N}_4\text{O}_2$.

4 The silicon oxynitride can be formed by exposing silicon nitride
5 portion 38 to an atmosphere comprising oxygen. The oxygen can be in
6 the form of, for example, one or more of ozone, NO or N_2O . Methods
7 for utilizing an atmosphere comprising oxygen to form silicon oxynitride
8 over silicon nitride portion 30 include, for example, plasma-enhanced
9 chemical vapor deposition, rapid thermal processing, high pressure
10 oxidation and low pressure oxidation. For the purposes of interpreting
11 this disclosure and the claims that follow, high pressure oxidation is
12 defined as oxidation occurring at pressures of 1 atmosphere and above,
13 and low pressure oxidation is defined as oxidation occurring at pressures
14 of less than 1 atmosphere. Example temperatures for forming silicon
15 oxynitride by high pressure oxidation are from about 600° C to about
16 900° C, and example temperatures forming silicon oxynitride by low
17 pressure oxidation are from about 700° C to about 1000° C. Example
18 conditions for forming silicon oxynitride by rapid thermal processing
19 comprise a temperature of from about 700° C to about 1000° C and a
20 ramp rate of from about 20 °C/second to about 100 °C/second.

21 If the silicon oxynitride is formed by chemical vapor deposition of
22 silicon, oxygen, and nitrogen, it can be formed in a common and
23 uninterrupted chemical vapor deposition process with portion 38. For

1 example, portion 38 can be formed in a CVD reaction chamber from a
2 first ratio of a silicon precursor gas and a nitrogen precursor gas.
3 Subsequently, an oxygen precursor gas can be introduced into the
4 reaction chamber. The oxygen precursor gas, silicon precursor gas and
5 nitrogen precursor gas can, in combination, form a silicon oxynitride
6 portion 40 over silicon nitride portion 38.

7 Referring to Fig. 6, a photoresist 42 is formed over silicon nitride
8 layer 36. In the shown preferred embodiment, there is no antireflective
9 coating formed between silicon nitride layer 36 and photoresist 42.
10 Instead, photoresist 42 is formed directly against upper portion 40 of
11 silicon nitride layer 36.

12 Referring to Fig. 7, photoresist 42 is exposed to a patterned beam
13 of light to render portions of photoresist 42 more soluble in a solvent
14 than other portions. The more soluble portions are then removed with
15 the solvent to pattern photoresist 42.

16 During the exposure of photoresist 42 to the beam of light,
17 portion 40 of silicon nitride layer 36 can be an antireflective surface.
18 It is found that a refractive index of a silicon nitride material increases
19 as the stoichiometric amount of silicon within the material is increased.
20 Silicon nitride materials having stoichiometries of Si_xN_y , wherein x is
21 greater than or equal to y , have refractive indices of greater than or
22 equal to about 2.2. Such silicon nitride materials can effectively function
23 as antireflective coatings. In contrast, traditional silicon nitride materials

1 (i.e., silicon nitride materials having stoichiometries of Si_3N_4) have
2 refractive indices of less than 2.0, and do not function as effective
3 antireflective surfaces.

4 Referring to Fig. 8, the pattern of photoresist 42 is transferred to
5 silicon nitride layer 36 and pad oxide 34 to form stacks 44 comprising
6 pad oxide 34, silicon nitride 36 and patterned photoresist 42. The
7 transferring of a pattern from photoresist 42 to layers 34 and 36 can
8 comprise, for example, an etch utilizing NF_3 and HBr . The susceptibility
9 of a silicon nitride layer to etching generally decreases as the silicon
10 nitride layer becomes more enriched with silicon. Thus, the removability
11 of a silicon nitride layer can be adjusted by adjusting the relative
12 proportions of silicon enriched portions to non-silicon enriched portions.
13 Specifically, silicon nitride layers having a higher proportion of less
14 silicon enriched portions to heavily silicon enriched portions can be
15 easier to remove in subsequent wafer processing. Example etch
16 conditions which proceed slower with respect to an silicon enriched
17 silicon nitride relative to a silicon nitride having a lower stoichiometric
18 amount of silicon are etching in hot phosphoric acid, or etching in dilute
19 hydrofluoric acid (wherein "dilute" refers to a hydrofluoric acid solution
20 comprising less than 50% hydrofluoric acid (by weight)).

21 In subsequent processing which is not shown, photoresist 42 can
22 be removed from over stacks 44. Additional processing can be utilized
23

1 to form field oxide between stacks 44, or to form conductive materials
2 electrically isolated by the insulative stacks 44.

3 Other embodiments of the invention are described with reference
4 to Figs. 9-15. Referring first to Figs. 9-12, and initially to Fig. 9, a
5 semiconductor wafer fragment in process is indicated generally with
6 reference numeral 110. Such includes a substrate composed of a bulk
7 monocrystalline silicon substrate 112 and an overlying insulating
8 layer 114, such as SiO_2 . An example thickness for layer 114 is from 50
9 Angstroms to 300 Angstroms.

10 Referring to Fig. 10, an outer layer 116 of Si_3N_4 is provided
11 outwardly of substrate 112/114. Nitride layer 116 includes an outer
12 surface 118. Thickness of layer 116 will depend upon the application.
13 For example where layer 116 is merely functioning as an etch stop in
14 some later process step, its thickness may approximate 100 Angstroms or
15 less. Where layer 116 is being used as a mask for a local oxidation of
16 silicon (LOCOS), layer 116 thickness may be from 1500 Angstroms to
17 3000 Angstroms.

18 The preferred manner of depositing or otherwise providing nitride
19 layer 116 is by chemical vapor deposition within a chemical vapor
20 deposition reactor using a gaseous silicon containing precursor and a
21 gaseous nitrogen containing precursor. An example preferred nitride
22 precursor is dichlorosilane (DCS), with a preferred nitrogen containing
23 precursor being ammonia (NH_3). One example set of deposition

1 parameters includes maintaining reactor temperature and pressure at
2 780°C and 250 mTorr, respectively, with the precursors being provided
3 at a volumetric ratio of DCS:NH₃ at 1:3. Such is but one example set
4 of conditions effective to deposit a Si₃N₄ layer on substrate 114/112.

5 Referring to Fig. 11, the gas flow of the nitrogen containing
6 precursor to the chemical vapor deposition reactor is reduced, thus
7 increasing the concentration of the silicon component of the precursor.
8 This will have the effect of enrichening the Si₃N₄ layer outermost surface
9 118 to outermost surface 118a with silicon atoms, as depicted by the
10 dots in the Fig. 11, to provide increased silicon concentration beyond the
11 empirical stoichiometric relationship of silicon to nitride atoms in
12 molecular silicon nitride. Thus, the outer silicon nitride surface has
13 been transformed into a material (i.e. silicon enriched Si₃N₄) which can
14 effectively be used to promote subsequent adhesion of photoresist to
15 Si₃N₄ layer 116a. Silicon is a material to which photoresist will more
16 readily adhere than Si₃N₄. An example reduction from the 1:3 DCS:NH₃
17 ratio to achieve such enrichening is to a ratio of from 1:0 to 1:1.25.

18 Referring to Fig. 12, a layer of photoresist is deposited over
19 silicon enriched outer Si₃N₄ surface 118a, and is for example patterned
20 as shown to produce photoresist blocks 120. Silicon enriched outer
21 surface 118a can optionally be treated with suitable other adhesion
22 primers appropriate to silicon, such as HMDS. Regardless, a desired
23 result is photoresist material 120 adhering to Si₃N₄ layer 116a with a

1 greater degree of adhesion than would otherwise occur if the outer Si_3N_4
2 surface 118 were not transformed by silicon enrichening. All of the
3 above described processing preferably and advantageously occurs in the
4 same single chemical vapor deposition reactor. Alternately, more than
5 one reactor chamber can be used.

6 An alternate embodiment 122 is described with reference to
7 Figs. 13 and 14. Such comprises a substrate composed of bulk
8 monocrystalline silicon 124 and an overlying SiO_2 layer 126. An outer
9 predominantly nitride layer 128 is provided over SiO_2 layer 126. Such
10 also includes an outer surface 130, the immediately underlying portion
11 thereof which has been transformed to an oxidized material 132,
12 preferably SiO_2 . Bulk mass 134 of layer 128 constitutes Si_3N_4 . The
13 processing to produce materials 134 and 132 preferably is again
14 conducted in a single, common chemical vapor deposition reactor.

15 Material 132 relative to outer surface 130 is preferably provided
16 by feeding a gaseous oxygen containing precursor to the reactor under
17 conditions effective to oxidize Si_3N_4 material 134 to SiO_2 material 132.
18 One example process for accomplishing such transformation of outer
19 surface 130 is to cease feeding the dichlorosilane and ammonia
20 precursors as described in the above example, and purging the reactor
21 of such gaseous precursors. Immediately thereafter, N_2O , O_2 , O_3 , or
22 mixtures thereof are fed to the reactor under the same temperature and
23 pressure conditions which effectively causes the outer surface of the

1 nitride material to become oxidized to SiO_2 . The thickness of material
2 132 is preferably kept very low, such as from about 10 Angstroms to
3 about 30 Angstroms. Purging of the Si_3N_4 precursors is highly desirable
4 to prevent an undesired silicon dust from falling out onto the wafer as
5 may occur without purging, which neither produces the SiO_2 material of
6 this example, nor readily adheres to the underlying substrate.

7 An example processing for O_3 , would be at atmospheric or
8 subatmospheric pressure at a temperature of 600°C for from one to two
9 hours. For O_2 , an example oxidizing condition would be feeding both
10 O_2 and H_2 at atmospheric pressure and temperatures ranging from 800°C
11 to 1100°C for from 30 minutes to two hours.

12 Alternately but less preferred, the above processing could take
13 place in two separate chambers, with the wafer(s) being moved from one
14 to the other after provision of the nitride layer for subsequent provision
15 of the adhesion promoting layer.

16 Referring to Fig. 14, a layer of photoresist is deposited and
17 patterned to produce photoresist blocks 136, as in the first described
18 embodiment. The photoresist adheres to Si_3N_4 layer 128 with a greater
19 degree of adhesion than would otherwise occur if the outer Si_3N_4 surface
20 130 were not oxidized.

21 Other alternate examples are described with reference to Fig. 15,
22 illustrating a semiconductor wafer fragment 140. Such again comprises
23 a substrate composed of a bulk monocrystalline silicon substrate 142 and

1 overlying SiO_2 layer 144. An overlying layer 146 of Si_3N_4 is provided,
2 preferably as described above with respect to the other embodiments.
3 Nitride layer 146 has an outer surface 148. Subsequently, conditions are
4 provided within a chemical vapor deposition reactor to cover outer Si_3N_4
5 surface 148 with a discrete photoresist adhesion layer 150 having a
6 thickness of preferably from about 10 Angstroms to about 30 Angstroms.
7 Thus, an outer composite substrate layer 152 is provided which
8 predominantly comprises Si_3N_4 . Example and preferred materials for thin
9 discrete photoresist adhesion layer 150 are silicon or SiO_2 .

10 Silicon can be deposited by any typical or known process for
11 depositing polycrystalline silicon atop a semiconductor wafer. An
12 example and preferred method for providing layer 150 to constitute SiO_2
13 is to first purge the reactor after Si_3N_4 layer deposition, followed by
14 feeding of DCS and N_2O to the reactor under temperature conditions of
15 780°C and 250 mTorr at a volumetric ratio of DCS: N_2O of from 1:3 to
16 1:10. Subsequently provided photoresist will adhere to Si_3N_4 layer 152
17 with a greater degree of adhesion than would otherwise occur if the
18 intermediate silicon, SiO_2 , or other adhesion promoting layer were not
19 present.

20 In compliance with the statute, the invention has been described
21 in language more or less specific as to structural and methodical
22 features. It is to be understood, however, that the invention is not
23 limited to the specific features shown and described, since the means

1 herein disclosed comprise preferred forms of putting the invention into
2 effect. The invention is, therefore, claimed in any of its forms or
3 modifications within the proper scope of the appended claims
4 appropriately interpreted in accordance with the doctrine of equivalents.
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